

# Self-Catalyzed Ternary Core–Shell GaAsP Nanowire Arrays Grown on Patterned Si Substrates by Molecular Beam Epitaxy

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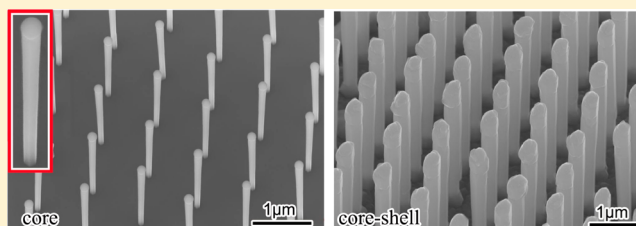
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**ABSTRACT:** The growth of self-catalyzed ternary core–shell GaAsP nanowire (NW) arrays on SiO<sub>2</sub> patterned Si(111) substrates has been demonstrated by using solid-source molecular beam epitaxy. A high-temperature deoxidization step up to ~900 °C prior to NW growth was used to remove the native oxide and/or SiO<sub>2</sub> residue from the patterned holes. To initiate the growth of GaAsP NW arrays, the Ga predeposition used for assisting the formation of Ga droplets in the patterned holes, was shown to be another essential step. The effects of the patterned-hole size on the NW morphology were also studied and explained using a simple growth model. A lattice-matched radial GaAsP core–shell NW structure has subsequently been developed with room-temperature photoluminescence emission around 740 nm. These results open up new perspectives for integrating position-controlled III–V NW photonic and electronic structures on a Si platform.

**KEYWORDS:** Nanowire array, patterned growth, self-catalyzed, GaAsP, III–V on Si, high-temperature deoxidization, molecular beam epitaxy



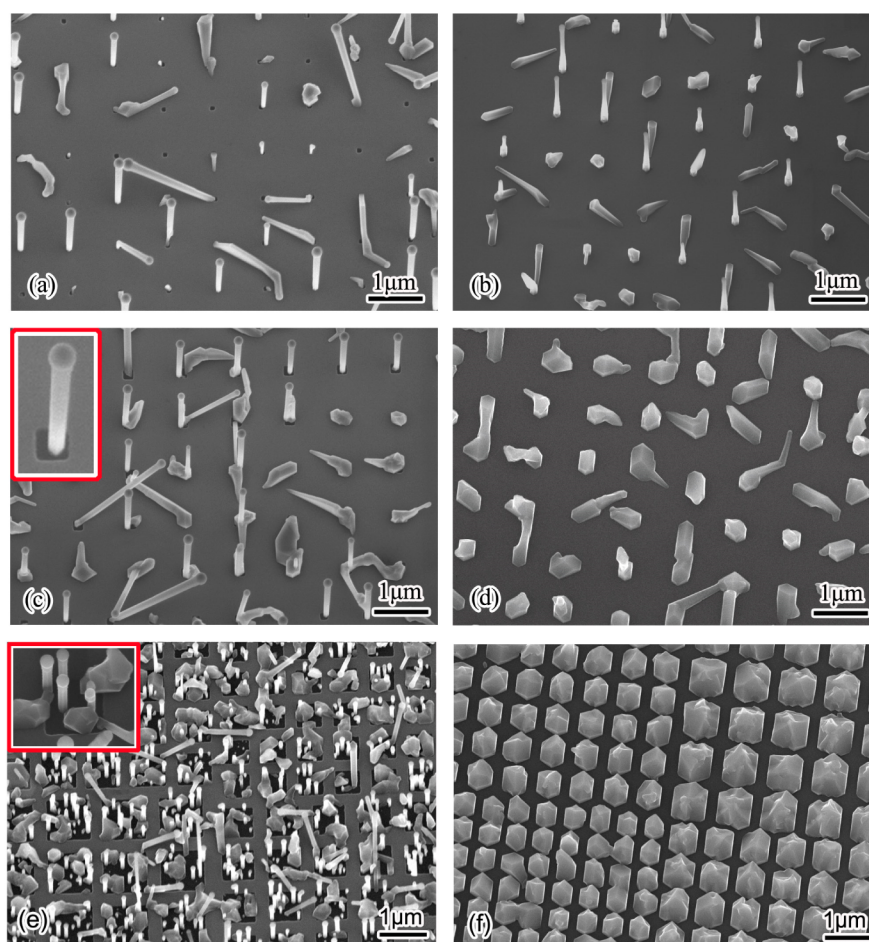
The integration of III–V materials on a Si platform has been pursued for more than 40 years.<sup>1,2</sup> By integrating the direct band gap III–V materials that have high absorption coefficients, high carrier mobilities, and large solar spectrum coverage onto the mature and cost-effective Si platform, it would create novel optoelectronic devices for Si photonics.<sup>3–9</sup> However, this integration remains challenging due to the large lattice mismatch and the difference in thermal expansion coefficient.<sup>3,10,11</sup> In recent years, one-dimensional semiconductor III–V nanowires (NWs) have gained significant attention for integrating III–V materials and devices on a Si platform because of their unique structural, optical, and electronic properties.<sup>12–15</sup> The strain formed between III–V NWs and Si substrates can be effectively relieved in an elastic way due to their small interfacial area.<sup>16–19</sup> The III–V materials could thus be monolithically grown on Si substrates in the form of NWs. At the same time, the novel device architectures with high performance have been predicted for III–V NWs monolithically grown on a Si platform.<sup>15,20–24</sup> For example, it has been predicted that a two-junction tandem solar cell (SC), consisting of a 1.7 eV NW junction and a 1.1 eV Si junction, has a theoretical efficiency of 33.8% at 1 sun AM1.5G and 42.3% under 500 suns AM1.5D concentration.<sup>25</sup> In addition, Scofield et al.<sup>26</sup> forecasted that a NW laser employing NW photonic crystal structure has the potential to have high-Q optical cavities, small mode volume, high spontaneous emission coupling factor, and low threshold power, which are highly desirable for photonic circuit integration.

The III–V NW growth on unpatterned substrates typically follows a self-assembled mechanism where the NWs are randomly positioned. To improve device performance, such as to achieve high-efficiency NW SCs<sup>27–29</sup> and to make NW photonic crystals,<sup>30,31</sup> each NW should be precisely located. Controlling the NW position is therefore of critical importance and can be achieved by growing on patterned substrates. Moreover, the parasitic bulk (cluster) deposition, often accompanying the NW growth on unpatterned substrates, can be suppressed by the pattern growth. Consequently, significant attention has been paid to the III–V NW growth on patterned substrates in recent years. Most are grown on GaAs, InAs, or InP substrates via selective area growth or gold-catalyzed growth.<sup>32–36</sup> The self-catalyzed growth method, by using Ga droplets in this work,<sup>37</sup> has the advantage of avoiding contamination associated with foreign metal catalytic droplets.<sup>38–40</sup> The Ga droplet can be crystallized into the NW to realize core–shell heterostructured NWs without any catalyzed vapor–liquid–solid (VLS)<sup>41</sup> growth of the shell material in the axial direction. More importantly, Ga-assisted NW growth tends to produce NWs with pure zinc blende phase and low defect densities due to the low surface energy and shape of the Ga droplet.<sup>21,42</sup> Despite the aforementioned benefits, there are

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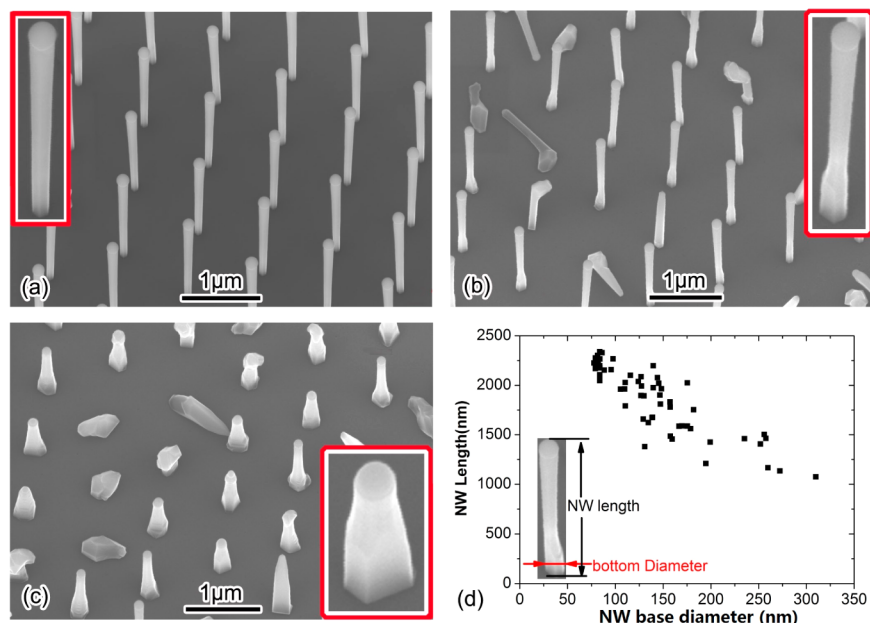


**Figure 1.** SEM images (tilt angle = 25°) of NWs grown on patterned substrates (a,c,e) without and (b,d,f) with the high-temperature deoxidization step. The measured sizes of holes are ~85 nm for (a,b), ~185 nm for (c,d), and between 500 nm and 1  $\mu\text{m}$  for (e,f). The insets in (c,e) show a magnified image of each patterned area.

only a few reports on self-catalyzed NW arrays on patterned Si substrates in the literature,<sup>28,43–47</sup> and it remains challenging and difficult to ensure reproducibility.<sup>28</sup>

Currently, III–V NW research is predominantly performed on binary material systems, such as GaAs and InAs, due to its simple fabrication procedures. Despite ternary NWs offering more freedom in adjusting the energy bandgap for different optoelectronic applications, it is a comparatively less touched field. The growth mechanism of ternary NWs is not well understood and many questions remain regarding the critical parameters of NW growth. There is only one report on self-catalyzed ternary III–V NWs grown on patterned Si substrates in the literature.<sup>43</sup> The ternary material, GaAsP, has a band gap that covers wavelengths ranging from green (550 nm) to near-infrared (860 nm) at room temperature.<sup>48</sup> Consequently, it is one of the most promising III–V compound semiconductors for photovoltaics and visible emitters. In this Letter, we demonstrated that a high-temperature deoxidization (HTD) step prior to NW growth is critical to thoroughly remove the oxide within the patterned holes for the growth of GaAsP NWs. To initiate the NW growth, a Ga predeposition step is another important step to assist the formation of Ga droplet. The influence of patterned-hole size on NW morphology has been further studied and explained. After the core GaAsP NW array growth, the growth of a lattice-matched GaAsP shell was finally demonstrated under vapor–solid (VS) epitaxial mode.

The patterned Si(111) substrates were prepared using nanoimprint lithography.<sup>46,49</sup> First, a layer of thermal oxide was grown in a high-temperature oven. SF2GS, microresist, was then spin coated over the oxide and imprinted with a jet-and-flash imprint lithography (Imprio 100) system. The imprinted patterns were transferred to the thermal oxide by depositing a 20 nm Al film as shadowing mask followed by both dry and wet etching of the thermal oxide. After the nanoimprint lithography, the patterned substrates were stored in ambient conditions before NW growth. Before being loaded into the ultrahigh-vacuum chamber of MBE system, a 5% aqueous hydrofluoric acid (HF) solution was used to chemically etch the substrates for 2 min in attempt to remove the native oxide from the patterned holes. The final mask SiO<sub>2</sub> thickness was ~30 nm, measured from transmission electron microscopy (TEM). The substrates were then rinsed with deionized water for 1 min and dried with nitrogen. After a thermal degassing at 500 °C for 1 h under ultrahigh vacuum conditions, the substrates were loaded into the MBE growth chamber for NW growth. For NW growth without the HTD step, the temperature was ramped directly to the growth temperature of ~630 °C. For NW growth with the HTD step, the substrates were heated up to 900 °C for 20 min and then cooled to a growth temperature of ~630 °C. The NWs were grown with a Ga flux of  $1.6 \times 10^{-7}$  Torr, V/III flux ratios between 3 and 20, and a P/(P + As) flux ratio of 12% throughout the growth duration of 45 min.



**Figure 2.** SEM images (tilt angle = 25°) of NWs grown in (a) ~50, (b) ~75, and (c) ~135 nm holes. (d) NW length as a function of NW base diameter for NWs shown in (a–c). The insets in panels a–c show the magnified images of a single NW grown in different-size patterned holes.

Scanning electron microscope (SEM) measurements of the nanowires were performed with a Zeiss XB 1540 FIB/SEM system.

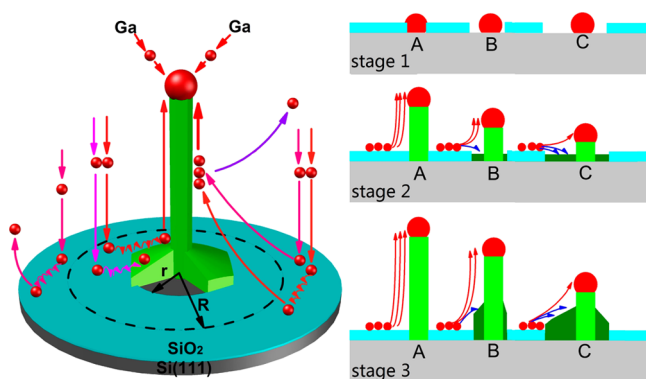
It is believed that the HF treatment can not only remove the native oxide layer but also form stable H-terminated Si surfaces.<sup>50–52</sup> The effect of using a HF solution to remove oxide in the patterned holes prior to the growth of GaAsP NWs was first investigated. The NW growth was initialized by simultaneously introducing Ga and group-V fluxes. For the samples without the HTD step, the patterned holes are only partially occupied by NW growth, as shown in Figure 1a,c,e. When the size of the patterned hole is ~85 nm, a significant number of patterned holes are vacant. For the occupied holes, there is only a single NW present, as shown in Figure 1a. For the wider holes (~185 nm), more holes are occupied by NWs and none is vacant as observed in Figure 1c. Further increasing the hole size to 0.5–1 μm, at least four NWs occupy each hole as observed in Figure 1e. A similar phenomenon has been reported previously.<sup>44,45,47</sup> These results suggest that the patterned holes in Figure 1a,c,e might be partly covered by the native oxide and/or SiO<sub>2</sub> residue prior to NW growth. To verify this, an in situ HTD step was used prior to the NW growth by heating the substrates up to ~900 °C to remove the native oxide and/or SiO<sub>2</sub> residue after the HF etch.<sup>3,5,53</sup> Figure 1b,d,f shows the effects of HTD step on NW growth. Although there are a few NWs grown in the smaller holes in Figure 1b, most of the holes are covered by clusters, and none is vacant as shown in Figure 1b,d,f. Considerable difference between the samples with and without the HTD step is that the patterned holes are completely occupied by III–V materials in the form of clusters or NWs for the samples with the HTD step, while for the samples without the HTD the patterned holes are partly occupied or vacant. This difference strongly suggests that native oxide and/or SiO<sub>2</sub> residue remain after the HF etch. If a thin oxide layer coats the patterned hole, pinholes, through which the Si lattice could be reached, may exist. The small pinhole size slows the Ga deposition rate and allows Ga adatoms to accumulate into a droplet and catalyze NW growth.<sup>54,55</sup> For

small patterned holes with the similar size of Ga droplets, the NW growth is limited to one, whereas multiple NWs could occupy the wider holes. Because of the inhibited III–V growth on the oxide layer, the position of the grown NW is determined by the pinhole position. Therefore, NWs only partially cover the holes, as shown in the insets of Figure 1c,e. An alternative explanation for the phenomenon in Figure 1a,c,e could be the reaction of Ga with the oxide layer to form pinholes in the patterned holes where NW growth initiates.<sup>56</sup> Both theories would explain the growth of NWs in Figure 1a,c,e, though a thin oxide layer remained because the Ga droplet could reach the Si substrate through a pinhole in the oxide. Consequently, the holes on the patterned substrate are likely not oxide-free after the HF cleaning. A thin oxide layer in patterned holes could be the reason for reduced repeatability and low yield reported previously for III–V NWs grown on patterned Si substrates.<sup>28</sup> This is also supported by the fact that the most successful patterned growths are reported on GaAs,<sup>31</sup> InAs,<sup>33</sup> or InP<sup>32</sup> substrates on which it is much easier to remove native oxide from patterned holes in comparison with Si substrates. For the samples with the HTD step, the native oxide and/or SiO<sub>2</sub> residue can be completely removed, leading to a fully exposed Si epitaxial surface for the patterned holes, and hence the complete filling of patterned holes with III–V materials as shown in Figure 1b,d,f. In Figure 1b, Ga consumption by VS epitaxial growth mode is slow because of the small hole size, which will allow a significant percentage of the Ga atoms to accumulate into a droplet and hence to catalyze the NW growth. However, for wider patterned holes in Figure 1d,f, the excessive nucleation area for GaAsP VS epitaxial growth rapidly consumes the Ga atoms and prevents droplet formation. This will inhibit the NW growth, leading to a cluster in each hole in Figure 1d,f. This suggests that an oxide layer on the Si substrate has a 2D nucleation-blocking effect that helps Ga adatoms accumulate into droplets for the self-catalyzed VLS growth.<sup>54,55</sup> It also indicates the importance of Ga droplet for self-catalyzed GaAsP NW growth.



To initiate the NW growth after the HTD step, a 60 s Ga predeposition step with a flux of  $1.6 \times 10^{-7}$  Torr was introduced to form Ga droplets before introducing group V fluxes. At the same time, the effects of hole sizes on the NW morphology were also studied, by having different patterned hole sizes (50, 75, and 135 nm) on the same Si growth substrate. For the small hole size ( $\sim 50$  nm), the NWs have a uniform morphology with a droplet on the tip of each NW (see Figure 2a), which confirms that the NW growth follows the catalyzed VLS growth mode. Increasing the hole size to  $\sim 75$  nm results in NW growth without uniform morphology and parasitic crystal growth observed at the NW base, as shown in the inset of Figure 2b. Further increasing hole size to  $\sim 135$  nm promotes the parasitic crystal growth and forms NWs with a wider base and stunted length, as shown in Figure 2c. The relationship between the NW base diameter and the NW length is summarized in Figure 2d. The NW length is decreased with increasing NW base diameter, which indicates that the parasitic crystal growth at the base of the NW is competitive with the NW growth.

The effects of hole size on the morphology of GaAsP nanowires could be explained by the size difference between the Ga droplets and patterned holes, which is illustrated by the three stages of NW growth in Figure 3. The first stage shows

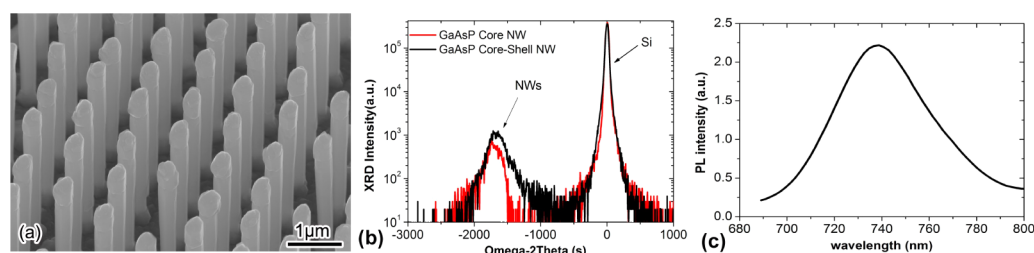


**Figure 3.** Illustration of the NWs grown in holes with different sizes at three stages: stage 1, the formation of Ga droplets; stage 2, the early stage of the NW growth; and stage 3, the final stage of the NW growth. The hole size in (A) is equal to or less than, (B) slightly greater than, and (C) much larger than the catalytic droplet size in stage 1.

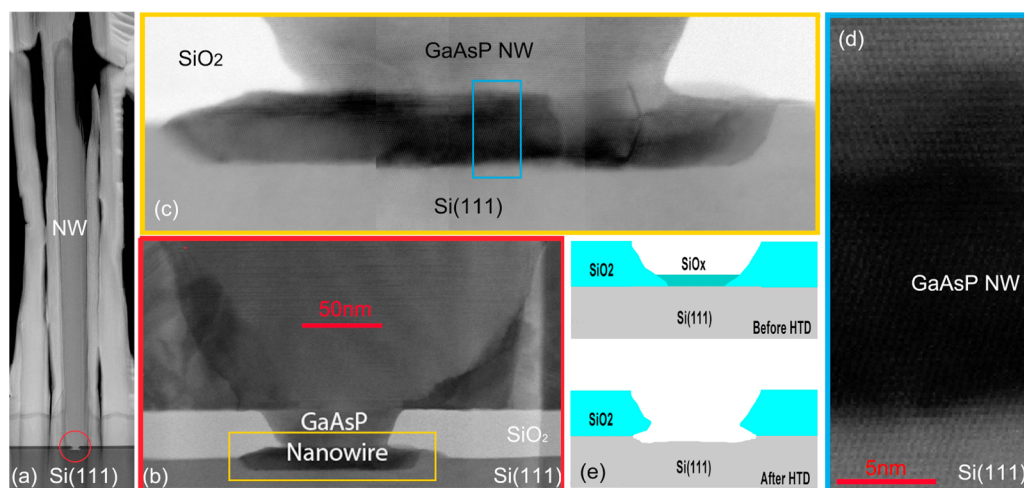
the formation of Ga droplets in the patterned holes using the Ga predeposition step. The droplet initiates NW VLS growth in the patterned holes.<sup>54</sup> Because the patterned holes in our research are oxide-free and their size is much less than the Ga adatom diffusion length at this temperature, there is a one-to-

one correspondence between holes and droplets. If the hole radius,  $r$ , is larger than that of the droplet, there will be a Si region that is not covered by the Ga droplet in the oxide-free hole, referred to as “vacant oxide-free area”. After the Ga predeposition in step 1, the group V flux is introduced with the group III flux to commence the NW growth at step 2. If the patterned-hole size is smaller than or equal to the droplet size, as shown in case A in Figure 3, all the Ga adatoms within the collection radius,  $R$ , are diffusing to the Ga droplet, which provides abundant Ga replenishment for the NW VLS growth. This is in accordance with the NW growth in  $\sim 50$  nm holes observed in Figure 2a. When the size of the patterned hole is slightly greater than the Ga droplet size, as shown in case B in Figure 3, there will be a vacant oxide-free Si area in the hole. In the presence of group V flux, the Ga adatoms are not only diffusing and incorporating into the droplet but also deposited together with As and P in the vacant oxide-free area in the form of VS epitaxial growth mode. The vacant oxide-free area will partially consume the Ga adatoms, leading to reducing the number of Ga adatoms incorporated into the droplet. As the NW growth proceeds, the VS epitaxial growth in the vacant oxide-free area grows along the NW length, which leads to the formation of the low energy side facets shown in Figure 2b. If the patterned-hole size is much greater than the catalytic droplet (see the case C in Figure 3), the vacant oxide-free area is much larger. As a result, most of the Ga adatoms diffusing from the  $\text{SiO}_2$  mask will be consumed by the VS epitaxial growth in the vacant oxide-free area. This will severely reduce the flux of Ga adatoms that reach the droplet for NW growth, leading to the formation of NWs with wide base and short length as observed in Figure 2c. This model also explains the reason why NWs that have a wider base diameter are shorter in length, as shown in Figure 2d.

Core-shell growth is highly desirable for NW applications as it not only adjusts the NW diameter but also permits the growth of an advanced structure by radial composition and doping modulation, such as p-i-n lateral junction and lateral quantum wells. Following the core NW growth, the Ga shutter was closed while keeping the group V fluxes to consume the Ga droplets. This leads to the termination of the axial growth. The GaAsP shell was then grown around the as-grown NWs by VS epitaxial growth mode at  $\sim 485^\circ\text{C}$  for 1 h with a Ga flux of  $1.6 \times 10^{-7}$  Torr, a V/III flux ratio of 60 and a P/(P + As) flux ratio of 30%. Figure 4a shows the SEM image of the core-shell GaAsP NWs. The core-shell NW array has uniform morphology with smooth sidewalls. The irregular tip is attributed to the core defects that originated during the unoptimized droplet consumption step for terminating the core growth. Figure 4b shows the X-ray diffraction of both the core and the core-shell NWs. The single-peak and close proximity



**Figure 4.** (a) SEM image of the core-shell GaAsP NW arrays (tilt angle =  $25^\circ$ ), (b) X-ray diffraction results of core and core-shell GaAsP NWs, and (c) room-temperature photoluminescence of the core-shell GaAsP NW arrays.



**Figure 5.** (a) Low-magnification TEM image of a core-shell NW standing vertically on the Si substrate. (b) TEM image of the interface between the NW and the Si substrate highlighted by the red circle in (a). (c) The magnified TEM image spliced from four images shows the interface area highlighted by the yellow box in (b). (d) High-resolution TEM image that shows the interface area highlighted by the blue box in (c). (e) Illustration of the high temperature desorption of oxide.

of the angles of their peak intensities indicate a lattice-matched core and shell for GaAsP NWs.<sup>37</sup> The optical properties of these core-shell NWs were also characterized at room temperature. The photoluminescence measurement was carried out with excitation from 635 nm diode-pumped solid-state laser at a power density of 500 mW/cm<sup>2</sup>. Figure 4c shows the room-temperature emission from the core-shell NW arrays with peak intensity at ~740 nm, which exhibits their good crystal quality and demonstrates their potential application in photovoltaics, visible emitters, and photonic crystals.

The interface between the core-shell NW and the Si substrate was studied with the use of TEM and is shown in Figure 5. As shown in Figure 5a,b, the NW is growing out of the patterned hole and standing vertically on the substrate. From Figure 5b–d, it is interesting to find out that the NW base is extended vertically into Si substrate and laterally wedged into the interface between the SiO<sub>2</sub> mask and the Si substrate. This phenomenon could be explained by the illustration in Figure 5e. During the HTD process, the high temperature will cause oxide evaporation. At the same time, the reaction between the Si and the oxide can also be triggered to produce SiO, which is much easier to evaporate than SiO<sub>2</sub> at this temperature.<sup>57</sup> The reaction started from the pinholes in the thin oxide layer in the holes and extended laterally along the Si/oxide interface, which caused an empty space wedged into the Si substrate below the patterned hole and the interface region between the SiO<sub>2</sub> mask and Si substrate. This wedged space into the Si substrate observed in Figure 5 indicates that the patterned holes are not free of the native oxide and/or SiO<sub>2</sub> residue prior to the HTD. During the NW growth, this empty wedged space will be filled by GaAsP.

In summary, the growth of self-catalyzed core-shell GaAsP NW arrays on patterned Si(111) substrates has been demonstrated by solid-source MBE. The chemical etching via HF solution is not sufficient to obtain oxide-free holes on the patterned substrates for the growth of III–V nanowires. By introducing an in situ high-temperature deoxidization step up to ~900 °C, the patterned holes can be thoroughly cleaned. Furthermore, the Ga predeposition step was demonstrated to be essential to the catalytic droplet formation in the oxide-free holes and hence ensure the NW growth via VLS growth mode

take place in the holes. The effects of the size of the patterned holes were also studied and shown to have a significant influence on the NW morphology. Finally, the growth of lattice-matched core-shell GaAsP NW arrays has been demonstrated with room-temperature PL emission around 740 nm. These results provide an essential step for the growth of ternary NW arrays on patterned Si substrates and offer us freedom in designing novel photonic devices by controlling both the ternary NW position and composition.

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### Notes

The authors declare no competing financial interest.

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